1. A method for making an integrated circuit using a patterned fill layer in kerf areas for more uniformly level process layers comprising the steps of:

providing a semiconductor substrate having an array of die areas for semiconductor devices, said array of die areas separated by said kerf areas;

(a) depositing a conducting layer on said substrate;

(b) patterning said conducting layer to form portions of said semiconductor devices in said die areas, and concurrently patterning said conducting layer in said kerf areas to form said patterned fill layer;

(c) depositing a spin-on-glass layer on said patterned conducting layer, wherein said patterned fill layer in said kerf areas provides a uniform coating over corners of said array of die areas without buildup of said spin-on-glass;

(d) curing said spin-on-glass layer;

(e) chemical-mechanical polishing back said spin-on-glass layer, wherein said fill layer prevents dishing in said kerf areas;

(f) depositing an insulating layer on said spin-on-glass layer;

(g) repeating steps (a) through (f) for each additional patterned conducting layer required to complete said integrated circuit.

2. The method of claim 1, wherein said conducting layer is a metal.

3. The method of claim 2, wherein said metal is aluminum deposited to a thickness of between about 5000 and 6000 Angstroms.

4. The method of claim 1, wherein spacing between said patterned fill layers and said die areas is not greater than about 2 micrometers.

5. The method of claim 1, wherein said kerf areas have a width of between about 120 and 600 micrometers between said die areas.

6. The method of claim 1, wherein said spin-on-glass layer is spin coated to a thickness of between about 3000 and 6000 Angstroms.

7. The method of claim 1, wherein said insulating layer is silicon oxide and is deposited by plasma enhanced chemical vapor deposition to a thickness of between about 4000 and 8000 Angstroms.

8. The method of claim 1, wherein said insulating layer is a borophosphosilicate glass deposited by

plasma enhanced chemical vapor deposition to a thickness of between about 4000 and 8000 Angstroms.

9. A method for making an integrated circuit using a patterned fill layer in kerf areas for more uniformly level process layers comprising the steps of:

providing a semiconductor substrate having an array of die areas for semiconductor devices, said array of die areas separated by said kerf areas;

(a) depositing a conducting layer on said substrate;

(b) patterning said conducting layer to form portions of said semiconductor devices in said die areas, and concurrently patterning said conducting layer in said kerf areas to form said patterned fill layer, wherein the space between said patterned fill layer and said die areas is not greater than 2 micrometers;

(c) depositing a spin-on-glass layer on said patterned conducting layer, wherein said patterned fill layer in said kerf areas provides a uniform coating over corners of said array of die areas without buildup of said spin-on-glass;

(d) curing said spin-on-glass layer;

(e) chemical-mechanical polishing back said spin-on-glass layer, wherein said fill layer prevents dishing in said kerf areas;

(f) depositing an insulating layer on said spin-on-glass layer;

(g) repeating steps (a) through (f) for each additional patterned conducting layer required to complete said integrated circuit.

10. The method of claim 9, wherein said conducting layer is a metal.

11. The method of claim 10, wherein said metal is aluminum deposited to a thickness of between about 6000 and 10000 Angstroms.

12. The method of claim 9, wherein said conducting layer is a polycide layer.

13. The method of claim 9, wherein said kerf areas have a width of between about 120 and 600 micrometers between said die areas.

14 The method of claim 9, wherein said spin-on-glass layer is spin coated to a thickness of between about 3000 and 6000 Angstroms.

15. The method of claim 9, wherein said insulating layer is silicon oxide and is deposited by plasma

enhanced chemical vapor deposition to a thickness of between about 4000 and 8000 Angstroms.

16. The method of claim 9, wherein said insulating layer is a borophosphosilicate glass deposited by plasma enhanced chemical vapor deposition to a thickness of between about 4000 and 8000 Angstroms.

17. The method of claim 9, wherein said integrated circuit is used to form a portion of a liquid crystal display.

18. A semiconductor substrate having an array of die areas with integrated circuits and kerf areas with fill patterns comprised of:

(a) a patterned conducting layer forming portions of semiconductor devices and a patterned fill layer in said kerf areas;

(b) a spin-on-glass layer over said patterned conducting layer, wherein said patterned fill layer in said kerf areas results in a uniform coating of said spin-on-glass layer over corners of said array of die areas, and said spin-on-glass layer converted to a silicon oxide by curing, and chemically-mechanically polished back to form a planar silicon oxide layer;

(c) an insulating layer on said silicon oxide layer;

the structure described in elements (a) through (c) formed for each additional patterned conducting layer, one upon the other, required for said integrated circuit.

19. The structure of claim 18, wherein said conducting layer is a metal.

20. The structure of claim 19, wherein said metal is aluminum deposited to a thickness of between about 6000 and 10000 Angstroms.

21. The structure of claim 18, wherein spacing between said patterned fill layers and said die areas is not greater than about 2 micrometers.

22. The structure of claim 18, wherein said kerf areas have a width of between about 120 and 600 micrometers between said die areas.